

REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2016 Course : Revised Course - 2013

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				IA	2	BC	Р			
	Digital Signal Proce	essors	& Embedded S	Systems						
				Theory	4	CC	P			
				IA	2	CC	P			
	Design for Testabil	ity & E-	Waste Manage	ement						
	,		-	Theory	4	CC	P			
				IA	2	BC	Р			
	Processor Architec	ture &	Parallel Proces	ssina						
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	Parallel Processing	y Lab		10	2	ВС	Р			
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NB WB HEIC 53

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2016 Course : Revised Course - 2013

COLLEGE:	GOA	COLLE	EGE (OF	ENGINEERING
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	ASIC Design & FPGA		Credits	Obta	ained	SGPA
	Alore Besign at Float	Theory	4	ВВ	Р	
		IA	2	AA	Р	
	Digital Signal Processors & Embedded		-	701		
		Theory	4	ВВ	Р	
		IA	2	ВВ	Р	
	Design for Testability & E-Waste Mana	gement				
	*	Theory	4	AB	P	
		IA	2	BC	Р	
	Processor Architecture & Parallel Proc	essing				
		Theory	4	FF	F	
		IA	2	BB	Р	
	Memory Design			9	14	
		Theory	4	AA	Р	
	Parallel Processing Lab	IA	2	AB	Р	6
	araner Processing Lab	IA	2	A.D.	_	
		Practical	2	AB CC	P P	
	FPGA & Embedded Systems Lab	ractical	2	CC	-	
	*	IA	2	ВВ	Р	
		Practical	2	BB	P	
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Of A	ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	Gran Obta BB BC CC BC BC BC BB BB	de nined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS PATIL ABHIJEET VILAS SGPA
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REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2016 Course : Revised Course - 2013

COLLECE.	COA	COLLEGE OF	ENGINEERING
CULLEGE.	GUA	COLLEGE OF	FIAGINFFULING

Seat No : 3215 PR No : 2	01007394 Sex	: M	Nam	ie:	SHETGAONKAR ANAY ANIL	
No Of Attempts: 1		No Of Credits	Grad Obtai		SGPA	*7
ASIC Design & FPGA						
	Theory	4	BC	P		
and the	IA	2	BB	P		
Digital Signal Processors & E	Embedded Systems				*	
	Theory	4	CC	P		
	IA	2	CC	Р		
Design for Teştability & E-Wa	aste Management					
,	Theory	4	FF	F		
	IA	2	CC	P		
Processor Architecture & Par	allel Processing					
	Theory	4	FF	F	20.00	
, r	IA	2	BC	P		
Memory Design					×	
	Theory	4	CC	Р		
	IA	2	CC	Р		
Parallel Processing Lab						
	IA	2	BB	Р		
	Practical	2	BC	P		
FPGA & Embedded Systems	Lab					
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ASIC Desig	n & FPGA						
		Theory	4	AA	Р		
		IA	2	AA	+		
Digital Sign	al Processors & Embedded	Systems					
		Theory	4	BC	P		8, E
		IA	2	BB	+		
Design for 7	Testability & E-Waste Manag	ement					
		Theory	4	AB	Р		
		IA	2	AA	+		
Processor A	Architecture & Parallel Proce	ssing					
2.		Theory	4	FF	F		
		IA	2	BB	+		
Memory De	sign						
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		IA	2	AA	+		HIVEA
Parallel Pro	cessing Lab						13/ 10/1
		IA	2	BC	+		(VALEREAD) =)
		Practical	2	ВС	+		A (PLAT AU 7
FPGA & En	nbedded Systems Lab						110000
		IA	2	AB	+		*
	· · · · · · · · · · · · · · · · · · ·	Practical	2	AB	+		A STATE OF THE PARTY OF THE PAR
		Total:	38			7.00 F	
						FAILS	

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
ВВ	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Checked By: Kul

Date: 13 10 16

S.S.J. Figueiredo
Assistant Registrar-E(Proff.)

Macedo Nacedo

Leo V. Macedo Controller Of Examinations Spring / 10/16

M. Shreedhara Offg. Registrar

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average