GOA UNIVERSITY
Established by State Legislature by Notification No.LD/10/7/84 (D) of 1984.
Taleigao Plateau, Goa – 403 206 INDIA.
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GU/Exam-Proff./M.E./May 2015/ 1115 Date: 12/10/2015

To,
The Principal,
Goa College of Engineering,
Farmagudi, Ponda-Goa.

Sub: **Revaluation result of Master of Engineering Examination held in May 2015.**

Sir,

This has reference to the applications for Revaluation made by the students of your college for the examination held in May 2015. In this connection please find below the grades after revaluation in the following subjects.

Seat No.	Subject	Grades before Revaluation	Grades after Revaluation
M.E. (E.T.C.)Microelectronics.			
	Semester II		
416	ASIC Design and FPGA	AA	AB
409	Digital Signal Processor and Embedded system	BB	CC
413	Digital Signal Processor and Embedded system	BB	BB
416	Digital Signal Processor and Embedded system	BB	BB
408	Design for testability and E-waste Management	BB	CC
409	Design for testability and E-waste Management	BC	CC
416	Design for testability and E-waste Management	AA	BC
408	Processor architecture and Parallel processing	BC	BC
409	Processor architecture and Parallel processing	CC	FF
410	Processor architecture and Parallel processing	FF	FF
414	Processor architecture and Parallel processing	FF	FF
416	Processor architecture and Parallel processing	BB	AB

GOA UNIVERSITY
Taleigao Plateau, Goa 403 206

REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
EXAMINATION HELD IN MAY 2015 Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 408 P R No : 201406597 Sex : F Name : DESAI SHRADDHA SADAGURU
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	AA	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	AB	P	
	IA	2	BB	P	
Design for Testability & E-Waste Management					
	Theory	4	BB	P	
	IA	2	AB	P	
Processor Architecture & Parallel Processing					
	Theory	4	BC	P	
	IA	2	AB	P	
Memory Design					
	Theory	4	AB	P	
	IA	2	AA	P	
Parallel Processing Lab					
	IA	2	AB	P	
	Practical	2	AB	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	P	
	Practical	2	AB	P	
	Total :	38			7.84 P
	NO CHANGE				PASSES

Seat No : 409 P R No : 200800913 Sex : F Name : DHARGALKAR SHRUTI RANGANATH
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	AB	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	BB	P	
	IA	2	BC	P	
Design for Testability & E-Waste Management					
	Theory	4	BC	P	
	IA	2	AA	P	
Processor Architecture & Parallel Processing					
	Theory	4	CC	P	
	IA	2	AB	P	
Memory Design					
	Theory	4	AB	P	
	IA	2	AB	P	
Parallel Processing Lab					
	IA	2	BB	P	
	Practical	2	BB	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	P	
	Practical	2	AB	P	
	Total :	38			7.26 P
	NO CHANGE				PASSES

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average

Discrepancy, if any in the Result shall be informed to the University within a week from the date of receipt of the result by the college

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REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
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COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 410 P R No : 201004714 Sex : F Name : KANADE SHRADDHA SABAJI
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA	
ASIC Design & FPGA						
	Theory	4	BC	P		
	IA	2	BB	P		
Digital Signal Processors & Embedded Systems						
	Theory	4	CC	P		
	IA	2	BC	P		
Design for Testability & E-Waste Management						
	Theory	4	CC	P		
	IA	2	CC	P		
Processor Architecture & Parallel Processing						
	Theory	4	FF	F		
	IA	2	BC	P		
Memory Design						
	Theory	4	FF	F		
	IA	2	BC	P		
Parallel Processing Lab						
	IA	2	BC	P		
	Practical	2	AB	P		
FPGA & Embedded Systems Lab						
	IA	2	AB	P		
	Practical	2	AA	P		
	Total :	38			4.89 F	Result Reserve
	NO CHANGE					Sem I Not Passed

Seat No : 413 P R No : 201008515 Sex : F Name : NAIK SHRUNKHALA SANTOSH
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	AB	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	BB	P	
	IA	2	AA	P	
Design for Testability & E-Waste Management					
	Theory	4	AB	P	
	IA	2	AB	P	
Processor Architecture & Parallel Processing					
	Theory	4	BB	P	
	IA	2	BB	P	
Memory Design					
	Theory	4	BB	P	
	IA	2	AA	P	
Parallel Processing Lab					
	IA	2	AA	P	
	Practical	2	AA	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	P	
	Practical	2	AA	P	
	Total :	38			7.95 P
					PASSES

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COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 414 P R No : 200800872 Sex : M Name : NORONHA ALWIN
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA	
ASIC Design & FPGA						
	Theory	4	BB	P		
	IA	2	BC	P		
Digital Signal Processors & Embedded Systems						
	Theory	4	FF	F		
	IA	2	CC	P		
Design for Testability & E-Waste Management						
	Theory	4	CC	P		
	IA	2	CC	P		
Processor Architecture & Parallel Processing						
	Theory	4	FF	F		
	IA	2	BB	P		
Memory Design						
	Theory	4	CC	P		
	IA	2	CC	P		
Parallel Processing Lab						
	IA	2	BC	P		
	Practical	2	BC	P		
FPGA & Embedded Systems Lab						
	IA	2	BB	P		
	Practical	2	BC	P		
	Total :	38			4.58 F	Result Reserve Sem I Not Passed

Seat No : 416 P R No : 201008295 Sex : F Name : PRABHU DESAI SANJANA SANTOSH
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA	
ASIC Design & FPGA						
	Theory	4	AA	P		
	IA	2	AA	P		
Digital Signal Processors & Embedded Systems						
	Theory	4	BB	P		
	IA	2	AB	P		
Design for Testability & E-Waste Management						
	Theory	4	AA	P		
	IA	2	AO	P		
Processor Architecture & Parallel Processing						
	Theory	4	AB	P		
	IA	2	AA	P		
Memory Design						
	Theory	4	AB	P		
	IA	2	AA	P		
Parallel Processing Lab						
	IA	2	AO	P		
	Practical	2	AO	P		
FPGA & Embedded Systems Lab						
	IA	2	AA	P		
	Practical	2	AO	P		
	Total :	38			8.74 P PASSES	

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REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
EXAMINATION HELD IN MAY 2015 Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 417 P R No : 200806910 Sex : M Name : SATARDEKAR GIRISH GURUDAS
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA	
ASIC Design & FPGA						
	Theory	4	BB	P		
	IA	2	BC	P		
Digital Signal Processors & Embedded Systems						
	Theory	4	CC	P		
	IA	2	CC	P		
Design for Testability & E-Waste Management						
	Theory	4	CC	P		
	IA	2	BC	P		
Processor Architecture & Parallel Processing						
	Theory	4	FF	F		
	IA	2	BB	P		
Memory Design						
	Theory	4	FF	F		
	IA	2	BB	P		
Parallel Processing Lab						
	IA	2	CC	P		
	Practical	2	BB	P		
FPGA & Embedded Systems Lab						
	IA	2	BB	P		
	Practical	2	BB	P		
	Total :	38			4.79 F	Result Reserve
	NO CHANGE					Sem I Not Passed

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
BB	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By : pphalo
Checked By : HW
Date : 29/10/15

S.S.J. Figueiredo
Assistant Registrar-E(Proff.)

Leo V. Macedo
Controller Of Examinations

Prof. V.P. Kamat
Registrar

GOA UNIVERSITY TALEIGAO PLATEAU GOA

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410	Memory Design	FF	FF
413	Memory Design	BC	BB
414	Memory Design	FF	CC
416	Memory Design	BB	AB
417	Memory Design	FF	FF

The tabulated Revaluation results will be sent to the college shortly.

Yours faithfully,

For CONTROLLER OF EXAMINATIONS