

GOA UNIVERSITY

Established by State Legislature by Notification No.LD/10/7/84 (D) of 1984.

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GU/Exam-Proff./M.E./May 2015/11/5

Date: 12/10/2015

To,
The Principal,
Goa College of Engineering,
Farmagudi, Ponda-Goa.

Sub: Revaluation result of Master of Engineering Examination held in May 2015.

Sir,

This has reference to the applications for Revaluation made by the students of your college for the examination held in ay 2015. In this connection please find below the grades after revaluation in the following subjects.

Seat No.	Subject	Grades before Revaluation	Grades after Revaluation
	M.E. (E.T.C.)Microelectro	nics.	
	Semester II		
416	ASIC Design and FPGA	AA	AB
409	Digital Signal Processor and Embedded system	n BB	CC
413	Digital Signal Processor and Embedded system	n BB	BB
416	Digital Signal Processor and Embedded system	n BB	BB
408	Design for testability and E-waste Management	BB	CC
409	Design for testability and E-waste Management	BC	CC
416	Design for testability and E-waste Managemen	t AA	ВС
408	Processor architecture and Parallel processing	BC	BC
409	Processor architecture and Parallel processing	CC	FF
410	Processor architecture and Parallel processing	FF	FF
414	Processor architecture and Parallel processing	FF	FF
416	Processor architecture and Parallel processing	BB	AB



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2015 Course : Revised Course - 2013

eat No: 408 PR No: 201406597	Sex	c: F	Nam	е: Г	DESAI SHRADDHA SADAGURU
o Of Attempts: 1		No Of	Grad		
		Credits	Obtai		SGPA
ASIC Design & FPGA					
	Theory	4	AA	Р	
	IA	2	AA	Р	
Digital Signal Processors & Embedded S					
	Theory	4	AB	Р	
	IA	2	BB	P	
Design for Testability & E-Waste Manag		0	192001	-	
	Theory	4	BB	P	
	IA .	2	AB	Р	
Processor Architecture & Parallel Proces		50			
	Theory	4	BC	P	
	IA	2	AB	Р	
Memory Design	1_1				
	Theory	4	AB	P	
	IA	2	AA	P	
Parallel Processing Lab		721		0-2400	
	IA	2	AB	Р	
	Practical	2	AB	Р	
FPGA & Embedded Systems Lab					
	IA	2	AB	Р	
	Practical	2	AB	Р	
	Total:	38			7.84 P
	NO CHAN				PASSES
eat No: 409 PR No: 200800913	Sex	k: F	Nam	ie: [DHARGALKAR SHRUTI RANGANATH
Of Attempts: 1		No Of	Grad		0004
ASIC Desire & EDGA		Credits	Obtai	ned	SGPA
ASIC Design & FPGA	TL		4.5	_	
	Theory	4	AB	Р	
Disital Cinnal Days and Control of the	IA	2	AA	Р	
Digital Signal Processors & Embedded S		*		-	
Digital Signal Processors & Embedded S	Theory	4	ВВ	Р	
	Theory IA	4 2	BB BC	P P	
Design for Testability & E-Waste Manag	Theory IA ement	2	ВС	Р	
	Theory IA ement Theory	2	BC BC	P P	
Design for Testability & E-Waste Manag	Theory IA ement Theory IA	2	ВС	Р	
	Theory IA ement Theory IA ssing	2 4 2	BC AA	P P P	
Design for Testability & E-Waste Manag	Theory IA ement Theory IA ssing Theory	2 4 2	BC BC AA CC	P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA ement Theory IA ssing	2 4 2	BC AA	P P P	
Design for Testability & E-Waste Manag	Theory IA ement Theory IA essing Theory IA	2 4 2 4 2	BC BC AA CC AB	P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA ement Theory IA ssing Theory IA Theory	2 4 2 4 2	BC BC AA CC AB	P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design	Theory IA ement Theory IA essing Theory IA	2 4 2 4 2	BC BC AA CC AB	P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA ement Theory IA ssing Theory IA Theory IA	2 4 2 4 2	BC BC AA CC AB AB	P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design	Theory IA ement Theory IA ssing Theory IA Theory IA Theory IA	2 4 2 4 2 4 2	BC BC AA CC AB AB AB	P P P P P	
Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA ement Theory IA ssing Theory IA Theory IA	2 4 2 4 2	BC BC AA CC AB AB	P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design	Theory IA ement Theory IA ssing Theory IA Theory IA IA Practical	2 4 2 4 2 4 2 2 2	BC BC AA CC AB AB AB BB	P P P P P P	
Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA ement Theory IA ssing Theory IA Theory IA Theory IA	2 4 2 4 2 4 2	BC BC AA CC AB AB AB	P P P P P	

M Bains

Practical

NO CHANGE

Total:

2

38

AB

7.26 P

PASSES



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2015 Course : Revised Course - 2013

Seat No: 410 PR No: 201004714	Sex	k: F	Nam	e :	KANADE SHRADDHA SABAJI
lo Of Attempts: 1		No Of Credits	Grad Obtai		SGPA
ASIC Design & FPGA				_	
	Theory	4	BC	Р	
D: 11 10: 1D 45 1 11 14	IA	2	BB	Р	
Digital Signal Processors & Embedded			00	_	
	Theory IA	4	CC BC	Р	
Design for Tootshility 9 E Wests Manag		2	ВС	Р	
Design for Testability & E-Waste Manag	Theory	4	CC	Р	
	IA	2	CC	Р	
Processor Architecture & Parallel Proce		2	CC	Г	
Frocessor Architecture & Parallel Froce	Theory	4	FF	F	
	IA	2	BC	P	
Memory Design	in	2	ь	Г	
Memory Design	Theory	4	FF	F	
	IA	2	BC	P	
Parallel Processing Lab	n.s.	-	50		
Talahor Tooddonig Lab	IA	2	ВС	Р	
	Practical	2	AB	P	
FPGA & Embedded Systems Lab	i idollodi	-	710		
Tr Great Emboured Systems Lab	IA	2	AB	Р	
	Practical	2	AA	P	
	Total:	38			4.89 F Result Reserve
	NO CHAN				Sem I Not Passed
eat No : 413 PR No : 201008515		x: F	Nam	ne :	NAIK SHRUNKHALA SANTOSH
o Of Attempts: 1		No Of	Gra		
		Credits	Obtai		SGPA
ASIC Design & FPGA					
	Theory	4	AB	P	
	IA	2	AA	Ρ	
Digital Signal Processors & Embedded	Systems				
	Theory	4	BB	Ρ	
	IA	2	AA	Ρ	
Design for Testability & E-Waste Manag	ement				
	Theory	4	AB	P	
	IA	2	AB	Ρ	
Processor Architecture & Parallel Proce					
	Theory	4	BB	Р	
	IA	2	BB	Р	
Memory Design					
	Theory	4	BB	Р	
	IA	2	AA	Ρ	
Parallel Processing Lab					
	IA	2	AA	Р	
	Practical	2	AA	Ρ	
FPGA & Embedded Systems Lab		NEG:			
	IA	2	AB	P	
	Practical	2	AA	Р	
	Total:	38			7.95 P
					PASSES

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
EXAMINATION HELD IN MAY 2015

Course: Revised Course - 2013

 COLLEGE: GOA COLLEGE OF ENGINEERING

 Seat No: 414
 P R No: 200800872
 Sex: M
 Name: NORONHA ALWIN

 No Of Attempts: 1
 No Of Credits
 Grade Obtained
 SGPA

 ASIC Design & FPGA
 Theory 4
 BB P

2 BC P Digital Signal Processors & Embedded Systems 4 FF F 2 CC Р Design for Testability & E-Waste Management Theory 4 CC P Р IA 2 CC Processor Architecture & Parallel Processing F Theory 4 FF BB Ρ IA 2 Memory Design CC P Theory 4 CC P IA 2 Parallel Processing Lab Р 2 BC IA Practical Р 2 BC FPGA & Embedded Systems Lab 2 BB Ρ IA

Practical 2 BC Р Total: 38 4.58 F Result Reserve Sem I Not Passed PRNo: 201008295 Sex: F Name: PRABHU DESAI SANJANA SANTOSH Seat No: 416 No Of Attempts: 1 No Of Grade **SGPA** Credits Obtained ASIC Design & FPGA Theory AA P 2 AA P Digital Signal Processors & Embedded Systems Theory 4 BB P 2 AB P Design for Testability & E-Waste Management Theory 4 AA P IA 2 AO P Processor Architecture & Parallel Processing P Theory 4 AB IA 2 AA P Memory Design Р Theory 4 AB IΑ 2 AA P Parallel Processing Lab IA 2 AO P Practical 2 AO P FPGA & Embedded Systems Lab 2 P IA AA Practical 2 AO P Total: 38 8.74 P

PASSES

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
EXAMINATION HELD IN MAY 2015

Course: Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING

Seat No: 417	PRNo: 200806910	Se	x: M	Nam	ne:	SATARDEKAR GIRISH GURUDAS
No Of Attempts: 1			No Of Credits	Grad Obtai		SGPA
ASIC Design	& FPGA					
		Theory	4	BB	P	
		IA	2	BC	P	
Digital Signal	Processors & Embedded S	Systems				
		Theory	4	CC	P	
		IA	2	CC	Р	
Design for Te	stability & E-Waste Manage	ement				
		Theory	4	CC	P	
		IA	2	BC	P	
Processor Are	chitecture & Parallel Proces	ssing				
		Theory	4	FF	F	
		IA	2	BB	Р	
Memory Desi	gn					
		Theory	4	FF	F	
		IA	2	BB	P	
Parallel Proce	essing Lab					
		IA	2	CC	P	
		Practical	2	BB	P	
FPGA & Emb	edded Systems Lab					
		IA	2	BB	Р	
		Practical	2	ВВ	Р	
		Total:	38			4.79 F Result Reserve
		NO CHAI	NGF			Sem I Not Passed

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
ВВ	7	Good
ВС	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By: pholo

Checked By :

Date: 29/10/15

S.S.J. Figueiredo
Assistant Registrar-E(Proff.)

Leo V. Macedo Controller Of Examinations Prof. V.P. Kamat Registrar



410	Memory Design	FF	FF
413	Memory Design	BC	BB
414	Memory Design	FF	CC
416	Memory Design	BB	AB
417	Memory Design	FF	FF

The tabulated Revaluation results will be sent to the college shortly.

Yours faithfully,

For CONTROLLER OF EXAMINATIONS