

REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II EXAMINATION HELD IN MAY 2017 Course: Revised Course - 2013

COLLEGE: GOA COLLEGE OF ENGINEERING Seat No: 3201 PRNo: 201203659 Sex: F Name: NAIK ASHIKA RAMAKANT No Of Attempts: 1 No Of Grade **SGPA** Credits Obtained ASIC Design & FPGA Theory 4 AΒ Р 2 IA AΑ P Digital Signal Processors & Embedded Systems Theory AB Р IΑ 2 AB Þ Design for Testability & E-Waste Management Theory AΑ IΑ 2 AO Р Processor Architecture & Parallel Processing Theory AΑ Р ΙA 2 AR Р Memory Design Theory 4 AA ΙA 2 AΑ P Parallel Processing Lab IΑ 2 AΒ Practical 2 ΑB Р FPGA & Embedded Systems Lab 2 IΑ Р BC Practical 2 Р AΑ Total: 38 8.47 P PASSES Seat No: 3202 PRNo: 201107721 Sex: F Name: PHADTE PRIYANKA DHARMA No Of Attempts: 1 No Of Grade **SGPA** Credits Obtained ASIC Design & FPGA Theory BC 4 Р 2 BB ľA Р Digital Signal Processors & Embedded Systems Theory 4 BB Ρ IΑ 2 BC Design for Testability & E-Waste Management Theory 4 BC P ŀΑ 2 AΒ Р Processor Architecture & Parallel Processing Theory 4 FF ΙΑ 2 CC Р

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Memory Design							
•	Theory	4	BC	P			
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Parallel Processing Lab							
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FPGA & Embedded Systems Lab							
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COLLEGE: GOA COLLEGE OF ENGINEERING

Seat No: 3203 PR No: 201611666		Sex: F		Name :		RASHINKAR PRAGATI GANAPATHI	
o Of Attempts: 1		No Of Credits			Grade Obtained		SGPA
ASIC Design	& FPGA		·		Oblu	11100	•
		Theory	4		BB	Ρ	
		IA	2		BB	Р	
Digital Signal	Processors & Embedded 8	Systems					
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		IA	2		BB	P	
Design for Te	stability & E-Waste Manag	ement					•
		Theory	4		CC	Р	
		IA ·	2		BC	Ρ	· ·
Processor Arc	chitecture & Parallel Proces	sing					
		Theory	4		FF	F	
		IA	2		CC	Р	
Memory Design	gn .						•
	•	Theory	.4		ΑŖ	Р	
		IA	2		AB	Ρ	
Parallel Proce	ssing Lab						
		IA	2		BC	Р	
		Practical	2		BC	Р	
FPGA & Embe	edded Systems Lab						
		IA	2		CC	Р	,
		Practical	2		BB	Р	
		Total: NO CHAN	38 IGE		Philipper to an industrial		5.74 F Result Reserve Sem I Not Passed
eat No: 3204	PRNo: 201107728	Se	x; F		Nam	е.	RODRIGUES FROILA VALENCY

				Sex: F		ne: F	RODRIGUES FROILA VALENCY		
No Of A	Attempts: 1 ASIC Design & FP	GΛ		No Of Credits	Gra Obta		SGPA		
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			IA	2	AA	Ρ			
	Digital Signal Proc	essors & Embedded S	Systems					•	
			Theory	4	BB	Ρ	•		
			IA	2	BB	٠P			
	Design for Testabil	ity & E-Waste Manage	ement	-					
		,	Theory	4	AB	Р			
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	Processor Architec	ture & Parallel Proces		-	7.0	'			
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ntservens ersten erst	ameri e jek emizzanu prano jamo jamo ja poveno i kaj jamajna jažijak (1) i kaj jek		Total:	38	- Meditable and particular		8.26 P PASSES	TALEIGAU PLATEAU	

Grade Grade Performance Points ΑO Outstanding 10 AΑ Excellent ΑВ Very Good 8 ВВ 7 Good BC6 Fair CC 5 Satisfactory

FF

Controller Of Examinations

Assistant Registrar-E(Proff.) P: Passes; F: Fails; A/ABS: Absent, N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average