



REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II  
EXAMINATION HELD IN MAY 2017  
Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3201 P R No : 201203659 Sex : F Name : NAIK ASHIKA RAMAKANT  
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	AB P	
	IA	2	AA P	
Digital Signal Processors & Embedded Systems	Theory	4	AB P	
	IA	2	AB P	
Design for Testability & E-Waste Management	Theory	4	AA P	
	IA	2	AO P	
Processor Architecture & Parallel Processing	Theory	4	AA P	
	IA	2	AB P	
Memory Design	Theory	4	AA P	
	IA	2	AA P	
Parallel Processing Lab	IA	2	AB P	
	Practical	2	AB P	
FPGA & Embedded Systems Lab	IA	2	BC P	
	Practical	2	AA P	
<b>Total :</b>		<b>38</b>		<b>8.47 P PASSES</b>

Seat No : 3202 P R No : 201107721 Sex : F Name : PHADTE PRIYANKA DHARMA  
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BC P	
	IA	2	BB P	
Digital Signal Processors & Embedded Systems	Theory	4	BB P	
	IA	2	BC P	
Design for Testability & E-Waste Management	Theory	4	BC P	
	IA	2	AB P	
Processor Architecture & Parallel Processing	Theory	4	FF F	
	IA	2	CC P	
Memory Design	Theory	4	BC P	
	IA	2	BB P	
Parallel Processing Lab	IA	2	BC P	
	Practical	2	BC P	
FPGA & Embedded Systems Lab	IA	2	CC P	
	Practical	2	AB P	
<b>Total :</b>		<b>38</b>		<b>5.68 F FAILS</b>

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REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II  
EXAMINATION HELD IN MAY 2017  
Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No: 3203 P R No: 201611666 Sex: F Name: RASHINKAR PRAGATI GANAPATHI  
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BB P	
	IA	2	BB P	
Digital Signal Processors & Embedded Systems	Theory	4	BC P	
	IA	2	BB P	
Design for Testability & E-Waste Management	Theory	4	CC P	
	IA	2	BC P	
Processor Architecture & Parallel Processing	Theory	4	FF F	
	IA	2	CC P	
Memory Design	Theory	4	AB P	
	IA	2	AB P	
Parallel Processing Lab	IA	2	BC P	
	Practical	2	BC P	
FPGA & Embedded Systems Lab	IA	2	CC P	
	Practical	2	BB P	
<b>Total :</b>		<b>38</b>	<b>5.74 F</b>	<b>Result Reserve Sem I Not Passed</b>
		<b>NO CHANGE</b>		

Seat No: 3204 P R No: 201107728 Sex: F Name: RODRIGUES FROILA VALENCY  
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA	Theory	4	BB P	
	IA	2	AA P	
Digital Signal Processors & Embedded Systems	Theory	4	BB P	
	IA	2	BB P	
Design for Testability & E-Waste Management	Theory	4	AB P	
	IA	2	AO P	
Processor Architecture & Parallel Processing	Theory	4	AB P	
	IA	2	AA P	
Memory Design	Theory	4	AB P	
	IA	2	AA P	
Parallel Processing Lab	IA	2	AA P	
	Practical	2	AA P	
FPGA & Embedded Systems Lab	IA	2	AA P	
	Practical	2	AO P	
<b>Total :</b>		<b>38</b>	<b>8.26 P</b>	<b>PASSES</b>

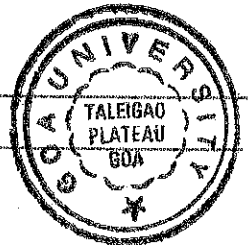
Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
BB	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By: *[Signature]*  
Checked By: *KM*  
Date: *17/10/17*

*[Signature]*  
Vivek Salaskar  
Assistant Registrar-E(Prof.)

*[Signature]*  
Prof. Anuradha Wagle  
Controller Of Examinations

*[Signature]*  
Y.V. Reddy  
Registrar



P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average

Discrepancy, if any in the Result shall be informed to the University within a week from the date of receipt of the result by the college